Electronic Version
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Claims

[c1] 1. A conductive memory device capable of storing information comprising:

a first electrode;

a first conductive metal oxide layer stacked upon and in electrical communication with the first electrode;

a second conductive metal oxide layer stacked upon and in electrical communication with the first conductive metal oxide layer;

a third conductive metal oxide layer stacked upon and in electrical communication with the second conductive metal oxide layer; and

a second electrode stacked upon and in electrical communication with the third conductive metal oxide layer; wherein the conductive memory element has a resistance that is indicative of the information stored therein.

[c2] 2. The conductive memory device of claim 1, wherein the first, second and third conductive metal oxide layers are substantially compatible.

[c3] 3. The conductive memory device of claim 1, wherein the first conductive layer is n-type or p-type, and the third

conductive layer is of opposite type.

[c4] 4. The conductive memory device of claim 1, wherein the first and third conductive layers are both of the same n-type or p-type, with different concentrations of mobile carriers.

[c5] 5. The conductive memory device of claim 1 wherein:

the resistance of the conductive memory element may be increased by applying a first voltage having a first polarity across the first and second electrodes and decreased by applying a second voltage having a second polarity across the conductive memory element.

[c6] 6. The conductive memory device of claim 5 wherein:

an initialization pulse across the first and second electrodes has no effect on establishing which polarity is needed to increase the resistance of the conductive memory element.

[c7] 7. The conductive memory device of claim 2 wherein:

the second conductive metal oxide layer has properties that differ from both the first conductive metal oxide layer and the third conductive metal oxide layer.

[c8] 8. The conductive memory device of claim 7 wherein:

the differences in properties between the conductive metal oxide layers determine the first polarity.

[c9] 9. The conductive memory device of claim 1, wherein: the first conductive metal oxide layer and the third conductive metal oxide layer are strontium titanate.

[c10] 10. The conductive memory device of claim 1, wherein: the first conductive metal oxide layer and the third conductive metal oxide layer are strontium zirconate.

[c11] 11. The conductive memory device of claim 10, wherein: the second conductive metal oxide layer is doped strontium zirconate.

[c12] 12. The conductive memory device of claim 11, wherein the second conductive metal oxide layer is doped with Chromium.

[c13] 13. The conductive memory device of claim 10, wherein: the first conductive metal oxide layer is strontium zirconate doped with an element with a higher valence than zirconium, such as niobium or tantalum, or doped with an element with a higher valence than strontium, such as yttrium or lanthanum.

[c14] 14. The conductive memory device of claim 10, wherein the third conductive metal oxide layer is strontium zir-

conate doped with an element that has a lower valence, such as iron or chromium.

[c15] 15. The conductive memory device of claim 1, wherein: the first conductive metal oxide layer and the third conductive metal oxide layer are praseodymium calcium manganese oxide ($Pr_xCa_{1-x}MnO_3$).

[c16] 16. The conductive memory device of claim 15, wherein: the first conductive metal oxide layer and the third conductive metal oxide layer do not have the same ratios of praseodymium to calcium.

[c17] 17. The conductive memory device of claim 1, wherein: the second conductive metal oxide layer is between 10 and 500 angstroms thick.

[c18] 18. The conductive memory device of claim 11, wherein: the second conductive metal oxide layer is about 30 angstroms thick.

[c19] 19. The conductive memory device of claim 1, wherein: the first conductive metal oxide layer and the third conductive metal oxide layer are each between 100 and 1000 angstroms thick

[c20] 20. The conductive memory device of claim 19, wherein: the first conductive metal oxide layer and the third

conductive metal oxide layer are each about 500 angstroms thick.

[c21] 21. The conductive memory device of claim 1, wherein: at least two of the first conductive metal oxide layer, the second conductive metal oxide layer, and the third conductive metal oxide layer have identical crystalline structures.

[c22] 22. The conductive memory device of claim 1, wherein: at least two of the first conductive metal oxide layer, the second conductive metal oxide layer, and the third conductive metal oxide layer have similar lattice parameters.

[c23] 23. The conductive memory device of claim 1, wherein: at least two of the first conductive metal oxide layer, the second conductive metal oxide layer, and the third conductive metal oxide layer have similar crystalline structures.

[c24] 24. The conductive memory device of claim 1, wherein: at least two of the first conductive metal oxide layer, the second conductive metal oxide layer, and the third conductive metal oxide layer have similar compositions.

[c25] 25. The conductive memory device of claim 1, wherein

the conductive memory element is rewriteable.

[c26] 26. The conductive memory device of claim 1, wherein:
at least one of the conductive metal oxide layers includes up to 10% dopant.

[c27] 27. A conductive memory device capable of storing information comprising:
a first electrode;
a first conductive metal oxide layer stacked upon and in electrical communication with the first electrode;
a second conductive metal oxide layer stacked upon and in electrical communication with the first conductive metal oxide layer; and
a second electrode stacked upon and in electrical communication with the second conductive metal oxide layer; wherein the conductive memory element has a resistivity that is indicative of the information stored therein.

[c28] 28. The conductive memory device of claim 27 wherein:
the resistivity of the conductive memory element may be increased by applying a first voltage having a first polarity across the first and second electrodes and decreased by applying a second voltage having a second polarity across the conductive memory element.

[c29] 29. The conductive memory device of claim 28 wherein:

an initialization pulse of the second polarity across the first and second electrodes has no effect on establishing which polarity is needed to increase the resistivity of the conductive memory element.

[c30] 30. The conductive memory device of claim 27 wherein:

the resistivity that is indicative of the information stored occurs in the first conductive metal oxide layer.

[c31] 31. The conductive memory device of claim 27 wherein:

either the first or second conductive metal oxide layer is strontium zirconate doped as n-type semiconductor; and

the remaining of the first or second conductive metal oxide layer is strontium zirconate doped as a p-type semiconductor.

[c32] 32. The conductive memory device of claim 27 wherein:

the resistivity that is indicative of the information stored occurs in the second conductive metal oxide layer.

[c33] 33. A method of manufacturing a conductive memory element comprising:

depositing a bottom conductive metal oxide layer;

depositing onto the bottom conductive metal oxide layer a top conductive metal oxide layer such that the top conductive metal oxide layer is in electrical communication with the bottom conductive metal oxide layer;

wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers; and

wherein the resistance of the conductive memory element can be modified during operation to store information.

[c34] 34. The method of manufacturing a conductive memory element of claim 33 wherein:

a continual sputtering process is used for depositing the bottom conductive metal oxide layer and the top metal oxide layer.

[c35] 35. The method of manufacturing a conductive memory element of claim 33 wherein the bottom and top conductive metal oxide layers are substantially compatible.

[c36] 36. The method of manufacturing a conductive memory element of claim 33, further comprising:

depositing onto the top conductive metal oxide layer a third conductive metal oxide layer such that the

third conductive metal oxide layer is in electrical communication with the top conductive metal oxide layer;

wherein either the bottom conductive metal oxide layer is a p-type material and the third conductive metal oxide layer is an n-type material, or the bottom conductive metal oxide layer is an n-type material and the third conductive metal oxide layer is a p-type material.

[c37] 37. The method of manufacturing a conductive memory element of claim 36, wherein:

a continual sputtering process is used for depositing the bottom conductive metal oxide layer, the top metal oxide layer and the third metal oxide layer.

[c38] 38. The method of manufacturing a conductive memory element of claim 36, wherein:

at least one of the bottom conductive metal oxide layer, the top conductive metal oxide layer, and the third conductive metal oxide layer contains a plurality of elements.

[c39] 39. The method of manufacturing a conductive memory element of claim 38, wherein:

the plurality of elements are co-sputtered.

[c40] 40. The method of manufacturing a conductive memory element of claim 36, wherein:

at least one of the bottom conductive metal oxide layer, the top conductive metal oxide layer, and the third conductive metal oxide layer further contains at least one dopant.

[c41] 41. The method of manufacturing a conductive memory element of claim 40, wherein

the at least one of the bottom conductive metal oxide layer, the top conductive metal oxide layer, and the third conductive metal oxide layer and the at least one dopant are co-sputtered.

[c42] 42. The method of manufacturing a conductive memory element of claim 36, further comprising:

ion implantation after depositing either the first bottom metal oxide layer, the top conductive metal oxide layer, or the third conductive metal oxide layer.

[c43] 43. The method of manufacturing a conductive memory element of claim 42, further comprising:

an anneal following the ion implantation.

[c44] 44. The method of manufacturing a conductive memory element of claim 36, further comprising:

an anneal after depositing the bottom conductive

metal oxide layer, the top conductive metal oxide layer, or the third conductive metal oxide layer.

[c45] 45. The method of manufacturing a conductive memory element of claim 33 wherein:

the manufacture of the conductive memory element is preceded by depositing at least one bottom electrode layer; and

the manufacture of the conductive memory element is followed by depositing at least one top electrode layer.